IN THE CLAIMS:

Rewrite the pending claims to read as follows:

1. (Currently Amended) A nonvolatile memory cell, comprising:

a high-voltage capacitor;

a high-voltage write path coupled to the high-voltage capacitor; and

a low-voltage read path coupled to both the high-voltage capacitor and the high-voltage write path;

wherein ~~either~~ the high-voltage write path is situated between the low-voltage read path and the high-voltage capacitor ~~or the high-voltage capacitor is situated between the low-voltage read path and the high-voltage write path~~.

2. (Original) The nonvolatile memory cell of claim 1 wherein the low-voltage read path comprises a floating gate transistor.

3. (Currently Amended) ~~The nonvolatile memory cell of claim 2~~

A nonvolatile memory cell, comprising:

a high-voltage capacitor;

a high-voltage write path coupled to the high-voltage capacitor; and

a low-voltage read path coupled to both the high-voltage capacitor and the high-voltage write path;

wherein either the high-voltage write path is situated between the low-voltage read path and the high-voltage capacitor or the high-voltage capacitor is situated between the low-voltage read path and the high-voltage write path;

wherein the low-voltage read path comprises a floating gate transistor; and

wherein the high-voltage capacitor comprises a conductive plate and a first diffusion region, wherein the conductive plate is separated from the first diffusion region by an oxide layer and is electrically connected to a floating gate of the floating gate transistor.

4. (Original) The nonvolatile memory cell of claim 3 wherein the high-voltage write path comprises a conductive plate and a second diffusion region, the conductive plate being electrically connected to the conductive plate of the high-voltage capacitor and at

least a portion of the conductive plate being separated from the second diffusion region by a layer of tunnel oxide.

5. (Original) The non-volatile memory cell of claim 2 wherein the floating gate transistor is a native floating gate transistor.

6. (Original) The nonvolatile memory cell of claim 2 wherein the low-voltage read path further comprises a read transistor.

7. (Original) The nonvolatile memory cell of claim 6 wherein the floating gate transistor and the read transistor are serially connected.

8. (Currently Amended) ~~The nonvolatile memory cell of claim 7~~

A nonvolatile memory cell, comprising:

a high-voltage capacitor;

a high-voltage write path coupled to the high-voltage capacitor; and

a low-voltage read path coupled to both the high-voltage capacitor and the high-voltage write path;

wherein either the high-voltage write path is situated between the low-voltage read path and the high-voltage capacitor or the high-voltage capacitor is situated between the low-voltage read path and the high-voltage write path;

wherein the low-voltage read path comprises a floating gate transistor and a read transistor serially connected to the floating gate transistor; and

wherein a diffusion region of the read transistor is electrically connected to a diffusion region of the floating gate transistor.

9. (Currently Amended) ~~The nonvolatile memory cell of claim 6~~

A nonvolatile memory cell, comprising:

a high-voltage capacitor;

a high-voltage write path coupled to the high-voltage capacitor; and

a low-voltage read path coupled to both the high-voltage capacitor and the high-voltage write path;

wherein either the high-voltage write path is situated between the low-voltage read path and the high-voltage capacitor or the high-voltage capacitor is situated between the low-voltage read path and the high-voltage write path;

wherein the low-voltage read path comprises a floating gate transistor and a read transistor; and

wherein the read transistor is significantly more resistive than the floating gate transistor when a read current runs serially through channels of the read transistor and the floating gate transistor.

10. (Currently Amended) A nonvolatile memory cell, comprising:

a high-voltage capacitor;

a high-voltage write path coupled to the high-voltage capacitor; and

a low-voltage read path coupled to both the high-voltage capacitor and the high voltage write path;

wherein the low-voltage read path includes a native floating gate transistor and the high-voltage write path is situated between the high-voltage capacitor and the low-voltage read path.

11. (Original) The nonvolatile memory cell of claim 10 wherein the high-voltage capacitor is situated between the low-voltage read path and the high-voltage write path.

12. (Original) The non-volatile memory cell of claim 10 wherein the high-voltage write path is situated between the low-voltage read path and the high-voltage capacitor.

13. (Currently Amended) ~~The nonvolatile memory cell of claim 10~~

A nonvolatile memory cell, comprising:

a high-voltage capacitor;

a high-voltage write path coupled to the high-voltage capacitor; and

a low-voltage read path coupled to both the high-voltage capacitor and the high voltage write path;

wherein the low-voltage read path includes a native floating gate transistor; and

wherein the high-voltage capacitor comprises a conductive plate and a first diffusion region, wherein the conductive plate is separated from the first diffusion region

by an oxide layer and is electrically connected to a floating gate of the floating gate transistor.

14. (Original) The nonvolatile memory cell of claim 13 wherein the low-voltage read path comprises a conductive plate and a second diffusion region, the conductive plate being electrically connected to the conductive plate of the high-voltage capacitor and at least a portion of the conductive plate being separated from the second diffusion region by a layer of tunnel oxide.

15. (Original) The nonvolatile memory cell of claim 10 wherein the low-voltage read path also includes a read transistor.

16. (Original) The nonvolatile memory cell of claim 15 wherein the floating gate transistor and the read transistor are serially connected.

17. (Currently Amended) ~~The nonvolatile memory cell of claim 16~~

A nonvolatile memory cell, comprising:

a high-voltage capacitor;

a high-voltage write path coupled to the high-voltage capacitor; and

a low-voltage read path coupled to both the high-voltage capacitor and the high voltage write path;

wherein the low-voltage read path includes a native floating gate transistor and a read transistor serially connected to the native floating transistor; and

wherein a diffusion region of the read transistor is electrically connected to a diffusion region of the floating gate transistor.

18. (Currently Amended) ~~The nonvolatile memory cell of claim 16~~

A nonvolatile memory cell, comprising:

a high-voltage capacitor;

a high-voltage write path coupled to the high-voltage capacitor; and

a low-voltage read path coupled to both the high-voltage capacitor and the high voltage write path;

wherein the low-voltage read path includes a native floating gate transistor and a read transistor serially connected to the native floating transistor; and

wherein the read transistor is significantly more resistive than the floating gate transistor when a read current runs serially through channels of the read transistor and the floating gate transistor.

19. (Currently Amended) A nonvolatile memory cell fabricated on a substrate, comprising:

a high-voltage capacitor having a first diffusion region in the substrate;

a high-voltage write path having at least a second diffusion region in the substrate; and

a low-voltage read path having at least a third diffusion region in the substrate;

wherein the second diffusion region is situated between the first diffusion region and the third diffusion region~~, or the first diffusion region is situated between the second diffusion region and the third diffusion region~~.

20. (Original) The nonvolatile memory cell of claim 19, further comprising a floating gate over the first diffusion region, the second diffusion region and the third diffusion region.

21. (New) A nonvolatile memory cell fabricated on a substrate, comprising:

a high-voltage capacitor on the substrate;

a high-voltage write path on the substrate; and

a low-voltage read path on the substrate;

wherein the high-voltage write path is sandwiched between the high-voltage capacitor and the low-voltage read path.

22. (New) The nonvolatile memory cell of claim 21, wherein the high-voltage capacitor is realized by a first diffusion region in the substrate, a first dielectric layer on the first diffusion region, and a first conductive plate on the first dielectric layer.

23. (New) The nonvolatile memory cell of claim 22, wherein the high-voltage write path includes a tunnel capacitor and a write-line transistor serially connected to the tunnel capacitor.

24. (New) The nonvolatile memory cell of claim 23, wherein the tunnel capacitor is realized by a second diffusion region in the substrate, a second dielectric layer on the second diffusion region and a second conductive plate on the second dielectric layer.

25. (New) The nonvolatile memory cell of claim 24, wherein the second dielectric layer is thinner than the first dielectric layer and the second conductive plate is electrically connected to the first conductive plate.

26. (New) The nonvolatile memory cell of claim 24, wherein the low-voltage read path includes a floating gate transistor and a read transistor serially connected to the floating gate transistor.

27. (New) The nonvolatile memory cell of claim 26, wherein the floating gate transistor has a gate terminal and the gate terminal is electrically connected to the first and second conductive plates.